1. (20%)  
The main memory of a computer is organized as 8 blocks (0..7). The cache has 4 block frames (0..3). Show the direct mapping, fully associative mapping, two-way set-associative mapping and sector mapping (2 blocks per sector) scheme.

2. (15%, 10%)  
A nonpipelined processor A has a clock rate of 25 MHz and an average CPI (cycles per instruction) of 5. Processor B, an improved successor of A, is designed with a five-stage linear instruction pipeline. The clock rate of B is 20 MHz.  
(a) If a program containing 100 instructions is executed on both processors, what is the speedup of processor B compared with that of processor A?  
(b) Calculate the MIPS rate of each processor during the execution of this particular program.

3. (4%, 4%)  
Explain the following terms as applied to communication patterns in a message-passing network:  
(a) Unicast versus multicast.  
(b) Broadcast versus conference.

4. (15%)  
If a floating-point adder has four-stage. Name the appropriate functions to be performed by the four stages.

5. (4%, 4%)  
Describe the fault-tolerant computer system of triple modular redundancy and design the "voter" circuit.

6. (15%, 8%)  
Consider a cache (M1) and memory (M2) hierarchy with the following characteristics:  
M1: 16K words, 50 ns access time  
M2: 1M words, 400 ns access time  
Assume eight-word cache blocks and a set size of 256 words with set-associative mapping:  
(a) Show the mapping between M2 and M1.  
(b) Calculate the effective memory access time with a cache hit ratio of h=0.98.