1. Please enumerate three types of pipeline hazards. (6%) 

2. For the following set of variables, \( \{CPI, \text{clock rate}, \text{cycle time}, \text{MIPS, I, C}\} \), please identify all of the subsets that can be used to calculate execution time. Each subset should be minimal; that is, it should not contain any variable that is not needed. For example, \( \{\text{MIPS, I}\} \) is one of the possible subsets. Let \( I = \text{number of instructions in program} \) and \( C = \text{number of cycles in program} \). (10%) 

3. Consider the computer with three instruction classes. Assume that the computer’s clock rate is 4 GHz. Suppose we measure the code for the same program from two different compilers and obtain the following data:

<table>
<thead>
<tr>
<th>CPI for this instruction class</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPI</td>
<td>2</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Code from</th>
<th>Instruction counts (in billions)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler 1</td>
<td>A 2 B 7 C 3</td>
</tr>
<tr>
<td>Compiler 2</td>
<td>A 1 B 2 C 2</td>
</tr>
</tbody>
</table>

(a) Which code sequence will execute faster according to execution time? Please explain your answer. (5%) 
(b) Which code sequence will execute faster according to MIPS? Please explain your answer. (5%) 

4. The following program tries to copy words from the address in register \( $a0 \) to the address in register \( $a1 \), counting the number of words copied in register \( $v0 \). The program stops copying when it finds a word equal to 0. You do not have to preserve the contents of the registers \( $v1, a0, \) and \( a1 \). This terminating word should be copied but not counted. (9%)

```
addi $v0, $zero, 0  # Initialize count
loop:  lw  $v1, 0($a0)  # Read next word from source
sw  $v1, 0($a1)  # Write to destination
addi $a0, $a0, 4  # Advance pointer to next source
addi $a1, $a1, 4  # Advance pointer to next destination
bne $v1, $zero, loop  # Loop if word copied is not zero
```

There are multiple bugs in this MIPS program; fix them and turn in a bug-free version.
5. For the following expression: \( A \times B - C / (D + E) + F \)
   (a) What is the prefix form of this expression? (5%)
   (b) What is the postfix form of this expression? (5%)

6. (a) Draw the final result after keys 20, 30, 10, 25, 15 are inserted into a max heap sequentially. (3%)
   (b) Draw the final result after an element is deleted from the max heap constructed in (a). (2%)
   (c) Draw the final result after keys 20, 30, 10, 25, 15 are inserted into a binary search tree sequentially. (3%)
   (d) Draw the final result after 10 is deleted from the binary search tree constructed in (c). (2%)

7. The following figure is an AOE (activity-on-edge) network with 11 activities \( a_1, a_2, \ldots, a_{11} \). The number associated with each activity is the time needed to perform that activity. For example, activity \( a_1 \) requires 6 days.
   (a) Please calculate the earliest start time \( e(i) \), and the latest start time, \( l(i) \), for activities \( a_6 \) and \( a_9 \). In other words, please calculate \( e(6) \), \( l(6) \), \( e(9) \), and \( l(9) \). (4%)
   (b) Which activities are critical? (4%)
   (c) What is the earliest time the project can finish? (2%)

8. Describe the actions taken by a kernel to switch context
   (a) Among threads (3%)
   (b) Among processes (3%)
9. Which of the following instructions should be privileged? (5%)
   a. Disable interrupts
   b. Read the system clock
   c. Set the time-of-day value
   d. Switch from user to monitor mode
   e. Jump to a user-defined function

10. Consider a demand paging system with three frames. The page reference sequence is given as follows:
    1, 4, 2, 5, 1, 5, 6, 7, 1, 7, 2, 7.
    How many page faults would occur for the following replacement algorithms? Note that all frames are initially empty. Please show your work.
    (a) LRU replacement (5%)
    (b) FIFO replacement (5%)
    (c) Optimal replacement (5%)

11. Assume you have a single processor system. The OS on the machine has a demand paged virtual memory system with a local replacement policy and a multi-level feedback queue (MLFQ) CPU scheduler. On the system there are two compute-intensive jobs running: Job-A and Job-B. Job-A has a large working set which results in frequent page faults. Job-B has a small working set and is able to reside in memory all the time. Assume you left the system to run for a while until it reached a steady state with both jobs running.
    (a) Which job would you expect to have a higher CPU scheduling priority from the MLFQ scheduler? Justify your answer. (4%)
    (b) Assume you switch from a local to a global replacement policy, how does this change affect the priorities of the jobs? Justify your answer. (5%)
    Hint: Global replacement allows a process to select a replacement frame from the set of all frames even if that frame is currently allocated to some other process. Local replacement requires that each process selects from only its own set of allocated frames.