[Closed book examination]

1. A virtual memory uses two-level page tables. The format of a virtual address is
   (table number, page number, displacement within page)

   The first four page tables are as follows:

   (a) For each of the following accesses to virtual memory, (8%)

   - If no page fault occurs, tell what physical address is computed. Give the answer in
     the form of (frame number, displacement).
   - Tell what access rights are needed to complete the access.

<table>
<thead>
<tr>
<th>Access</th>
<th>Table number</th>
<th>Page number</th>
<th>Displacement within page</th>
<th>Physical address</th>
<th>Access rights</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fetch data</td>
<td>1</td>
<td>2</td>
<td>50</td>
<td>page fault</td>
<td>read</td>
</tr>
<tr>
<td>Fetch data</td>
<td>0</td>
<td>1</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Store data</td>
<td>2</td>
<td>3</td>
<td>2000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jump to</td>
<td>3</td>
<td>3</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jump to</td>
<td>0</td>
<td>2</td>
<td>60</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

   (b) If all the above references are possible, how large is the virtual address space (at least)? (5%)

   How large is the physical memory (at least)? (5%)

2. Consider a machine on which 20 percent of the instructions are conditional jumps and
   another 10 percent are loop jumps. The conditional jumps can be predicted with 60 percent
   accuracy and the loop jumps can be predicted with 90 percent accuracy. The penalty for
   guessing wrong is four cycles. There is no penalty for unconditional jumps or correct
   guesses. What is the efficiency of the pipeline on this machine? (16%)

3. a. What is the bit stuffing scheme used in the bit oriented protocol? (4%)
   b. What is the character stuffing scheme used in the character oriented protocol? (4%)
   c. What is the actual data if the bit stream "011111001111011111101" is received? (4%)
   d. What is the data received while the actual character data is "DLE STX DLE DLE
      ETX DLE ETX DLE DLE ETX"? (4%)

命題題外
4. A computer system contains a main memory of 32K 16-bit words. It also has a 4K-word cache divided into 4-slot sets with 64 words per slot. Assume that the cache is initially empty. The CPU fetches words from locations 10, 11, 12, ..., 4220 in that order. It then repeats this fetch sequence 5 more times. The cache is 5 times faster than main memory. Estimate the improvement resulting from the use of the cache. Assume a FIFO policy for block replacement. (20%)

5. Consider the execution of the following program for the Tower of Hanoi on a RISC machine with overlapping windows. The main program uses a register window itself and calls TOWER(3, 2, 1) Then:
   (a) How many times does a window have to be saved in order to allow a call to complete if three windows are available? Why? (15%) 
   (b) Same question as (a) but with four windows? (5%) 
   procedure towers(n, i, j: integer); 
   var k: integer; 
   begin 
     if n = 1 then writeln('move a disk from peg', i, 'to peg', j) 
     else begin 
       k := 6 - 1 - j; 
       towers(n-1, i, k); 
       towers(1, i, j); 
       towers(n-1, k, j) 
     end; 
   end; (towers)

6. Produce a vectorized version of the following program. Show steps to justify your answer. (10%)

   DO 20 I = 3, N
   B(I, 1) = 0
   DO 10 J = 4, M
   A(I) = A(I) + B(I, J+1)
   10 CONTINUE
   C(I) = D(I) + E(I)
   D(I) = 2 * C(I + 1)
   20 CONTINUE